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A new metal demonstrated to form ideal rectifying Schottky diode junctions to n-type SiC, and further, not to limit the thermal and power density capability of SiC devices and circuits in any way. The following properties were demonstrated between RT and 1050 C: (1) metal does not spall, peel or scratch, (2) metal/n-SiC junction remains abrupt, (3) I-V unchanged by thermal exposure, (4) barrier height = 1.78+/-0.1 eV.

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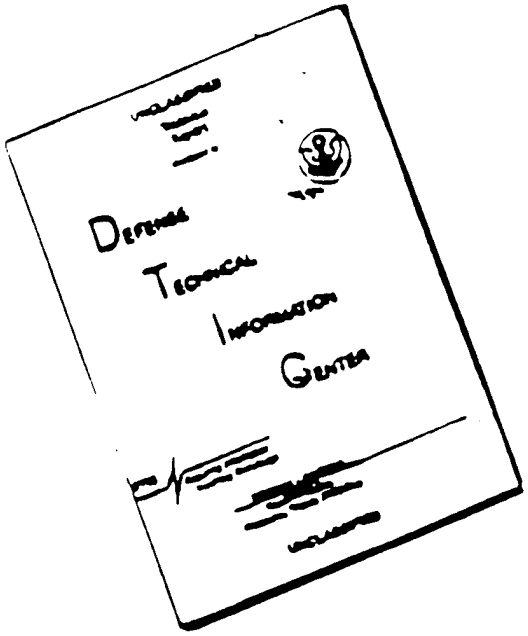


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## ABSTRACT

Requirements for revolutionary advances in solid state high temperature power electronics are the motivations for development of wide bandgap semiconductor device technology. The value of SiC for these applications accrues from its inherent potential to modulate very high voltages and current densities, and to operate reliably at very high temperatures. However, until now, SiC devices requiring n-type, rectifying Schottky junctions were limited to power densities and temperatures far below the capabilities of SiC itself. Such devices include: ultra-fast power rectifiers, MESFETs, mixer diodes and thermal sensors.

In this Phase I SBIR we proposed that Os would form a rectifying contact with n-type SiC that would be electrically superior to any other metal (or metal-silicide), and that its mechanical and thermal properties - in contact with SiC - would facilitate the application of n-type SiC Schottky junctions over the full power density and temperature range capabilities of SiC itself. The following characteristics were projected for Os and its rectifying junctions with n-type SiC: (1) a Schottky barrier higher than possible with any other metal; (2) outstanding adhesion, scratch and peel resistance regardless of the thermal stress conditions; and (3) an abrupt Os/SiC interface that remains stable to at least 1000°C.

The results presented in this report show that we were correct in all of our predictions. The average electrical properties of the Os Schottky junctions to n-type SiC were investigated using 6H-SiC substrates with doping concentrations of $10^{18}cm^{-3}$. This is the most demanding of all possible tests of the usefulness of Os as n-type rectifying contact, because if it works for such high concentrations, it will work for all lower concentrations. The barrier height (independent of doping) was determined to be 1.78 volts; this is the higher than Pt or Ti. The calculated work function voltage of Os, based on C-V measurements of the Os/n-SiC junction, is 5.91±0.1 volts. This is - within experimental error - equal to the published Os work function voltage of 5.93 volts; thus, indicating that the Os/SiC interface state density is very low.

The mechanical properties of Os in contact with SiC are superior in every respect, and they do not deteriorate under cycled or sustained thermal stress up to 1050°C. The Os/SiC junction remains abrupt at all temperatures below 1050°C, indicating that Os forms its junction with SiC by bonding to the exposed Si. However, we did determine that this bonding process creates less than 3 monolayers of free carbon, but this can be eliminated by deposition of a few monolayers of Si on SiC before depositing Os. In addition, we learned that Os forms a stable interface with silicon dioxide and that this interface and the mechanical properties of Os are equal to those of the Os/SiC junction. The abruptness and outstanding stability of Os/SiC and Os/$SiO_2$ junctions is illustrated in Fig. 14 of this report (included in the second page of this abstract).

The feasibility of Os / n-type SiC Schottky diodes was clearly demonstrated, and a foundation for development of full power/temperature range SiC devices with n-type Schottky junctions was established.

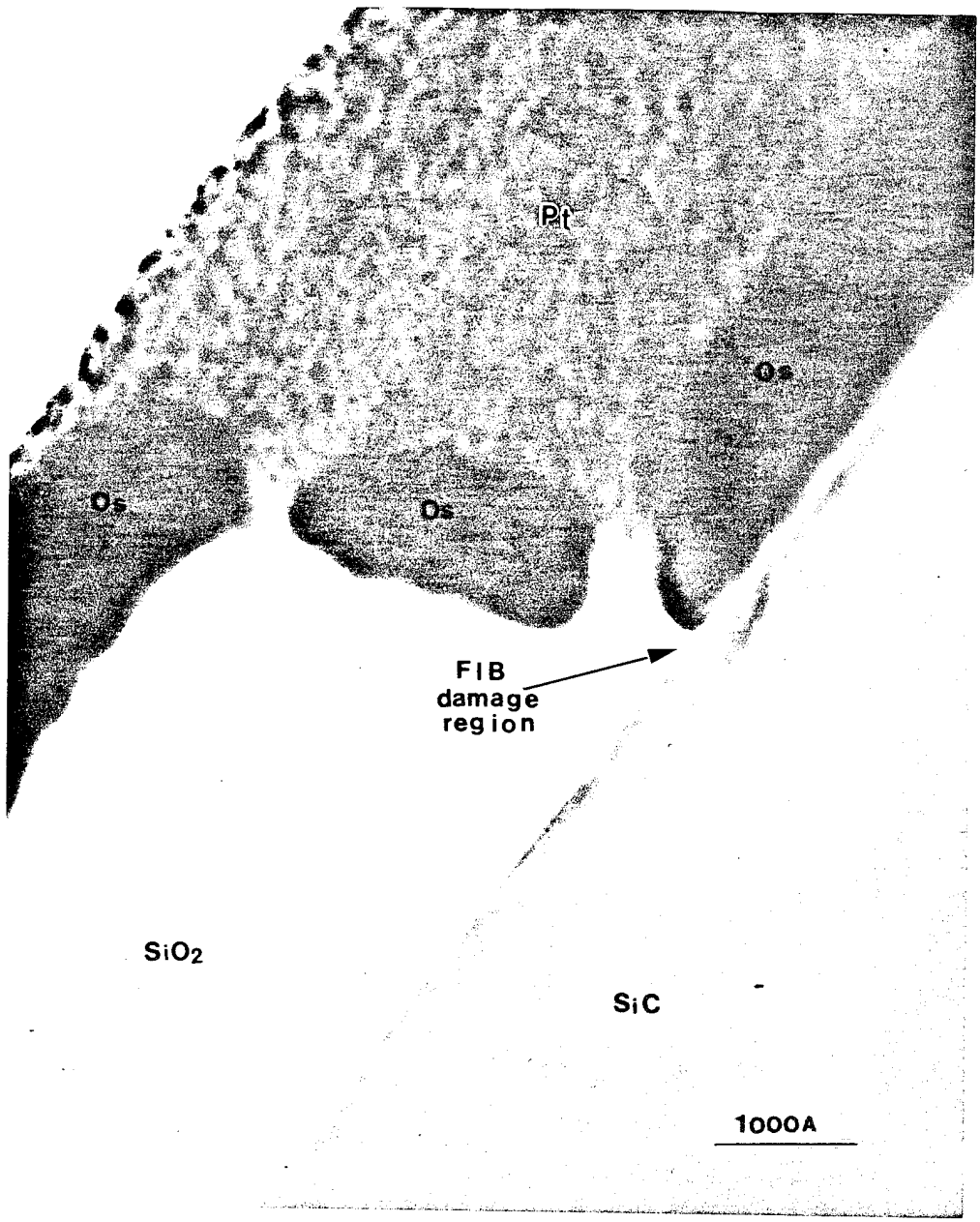



**Fig.14.** TEM cross-section of Os/SIC interface (left), Os/$SiO_2$ interfaces (upper center and right) and SiC/$SiO_2$ interface (center right). Several important features are shown in this x-sec. of sample D1 (annealed at 1050°C, as described in Table III):

1. Their are gaps in the as-sputtered Os, at the high curvature positions of the side wall of the $SiO_2$ field ring.
2. The effect of the FIB beam spreading on interface damage is clearly evidenced by observing that the white region between the Os and SiC also extends throughout the SiC/$SiO_2$ interface; where, significant FIB damage can be seen in the SiC at the SiC/Os/$SiO_2$ junction.
3. The interfaces formed with SiC do not show any evidence of chemical reaction.

## 1. Introduction

*Requirements for revolutionary advances in solid state high temperature power electronics are the motivations for development of wide bandgap semiconductor device technology. The value of SiC for these applications accrues from its inherent potential to modulate very high voltages and current densities, and to operate reliably at very high temperatures. However, until now, SiC devices requiring n-type, rectifying Schottky junctions were limited to power densities and temperatures far below the capabilities of SiC itself. Such devices include: ultra-fast power rectifiers, MESFETs, mixer diodes and thermal sensors.*

*In this Phase I SBIR we proposed that Os would form a rectifying contact with n-type SiC that would be electrically superior to any other metal (or metal-silicide), and that its mechanical and thermal properties - in contact with SiC - would facilitate the application of n-type SiC Schottky junctions over the full power density and temperature range capabilities of SiC itself. The following characteristics were projected for Os and its rectifying junctions with n-type SiC: (1) a Schottky barrier higher than possible with any other metal; (2) outstanding adhesion, scratch and peel resistance regardless of the thermal stress conditions; and (3) an abrupt Os/SiC interface that remains stable to at least 1000°C.*

*The results presented in this report show that we were correct in all of our predictions. The average electrical properties of the Os Schottky junctions to n-type SiC were investigated using 6H-SiC substrates with doping concentrations of $10^{18}cm^{-3}$. This is the most demanding of all possible tests of the usefulness of Os as n-type rectifying contact, because if it works for such high concentrations, it will work for all lower concentrations. The barrier height (independent of doping) was determined to be 1.78 volts; this is the higher than Pt or Ti. The mechanical properties of Os in contact with SiC are superior in every respect, and they do not deteriorate under cycled or sustained thermal stress up to 1050°C. The Os/SiC junction remains abrupt at all temperatures below 1050°C, indicating that Os forms its junction with SiC by bonding to the exposed Si. However, we did determine that this bonding process creates some free carbon, but this can be eliminated by deposition of one or more monolayers of Si on SiC before depositing Os. In addition, we learned that Os forms a stable interface with silicon dioxide and that this interface and the mechanical properties of Os are equal to those of the Os/SiC junction.*

*The feasibility of Os / n-type SiC Schottky diodes was clearly demonstrated, and a foundation for development of full power/temperature range SiC devices with n-type Schottky junctions was established.*

## 2. Properties of As-Deposited Structures

Osmium was RF sputtered onto fifteen 6H-SiC substrates by Communications and Power Industries (CPI). The substrates are identified by the type of Os pattern deposited on them.

Type 1. Os deposited over entire surface:

Sample # 1A, 1B and 1C (3 pieces of a single <0001> 6H-SiC substrate).
Sample # 2A and 2B (2 pieces of a single <0001> 6H-SiC substrate).
Sample # 3A and 3B (2 pieces of a single <0001> 6H-SiC substrate).
Sample # 4. (<0001> 6H-SiC substrate).

Type 2. Os diode arrays (Fig. 1).

Array = repeating pattern of diodes of the following dimensions:

- Size W: Diameter = 200 μm, Area = $3.14 \times 10^{-4}$ cm$^2$
- Size X: Diameter = 80 μm, Area = $5.03 \times 10^{-5}$ cm$^2$
- Size Y: Diameter = 40 μm, Area = $1.26 \times 10^{-5}$ cm$^2$
- Size Z: Diameter = 20 μm, Area = $3.14 \times 10^{-6}$ cm$^2$

Sample # A1, A2, A3, A4 and A5 (<0001> 6H-SiC substrates).

Type 3. Os vertical diode + field spreading ring arrays (Fig. 2):

Array = repeating pattern of diodes + rings of the following dimensions:

- Size W: Diode Diam = 200 μm Area = $3.14 \times 10^{-4}$ cm$^2$ Ring Annular Radius = 20 μm
- Size X: Diode Diam = 80 μm, Area = $5.03 \times 10^{-5}$ cm$^2$ Ring Annular Radius = 20 μm
- Size Y: Diode Diam = 40 μm, Area = $1.26 \times 10^{-5}$ cm$^2$ Ring Annular Radius = 20 μm
- Size Z: Diode Diam = 20 μm, Area = $3.14 \times 10^{-6}$ cm$^2$ Ring Annular Radius = 20 μm

Sample # D1 (<0001>3.5°off 6H-SiC substrate).
Sample # D2 (<0001> 6H-SiC substrate).

Physical and electrical characteristics of the as-deposited Os are summarized below.

Thickness: 900±50 Å, as measured by capacitance profilometer.

Surface morphology: Smooth and specular, as shown in Figs. 3a and 3b.

Adhesion during photo resist lift-off: The portion of as-deposited Os on the photo resist mask lifted off easily. The Os deposited on the SiC and $SiO_2$ surfaces did not peel, as shown in Figs. 3a and 3b.

Mechanical properties of the Os/SiC & Os/$SiO_2$ structures: The Os was very resistant to scratching by 2.4 μm diameter, spring loaded, tungsten (W) probes. Os surfaces could only be scratched by applying pressure well beyond that required to bend the probe tips. The Os dots could not be removed with Scotch tape.

Electrical properties of Os films and Os/n-SiC junctions: The average resistance - measured between 2.4 μm W probes, spaced approximately 100 μm apart - was 170 ohms. Junction properties are presented with thermal stress test data obtained from Type 2 and Type 3 structures.

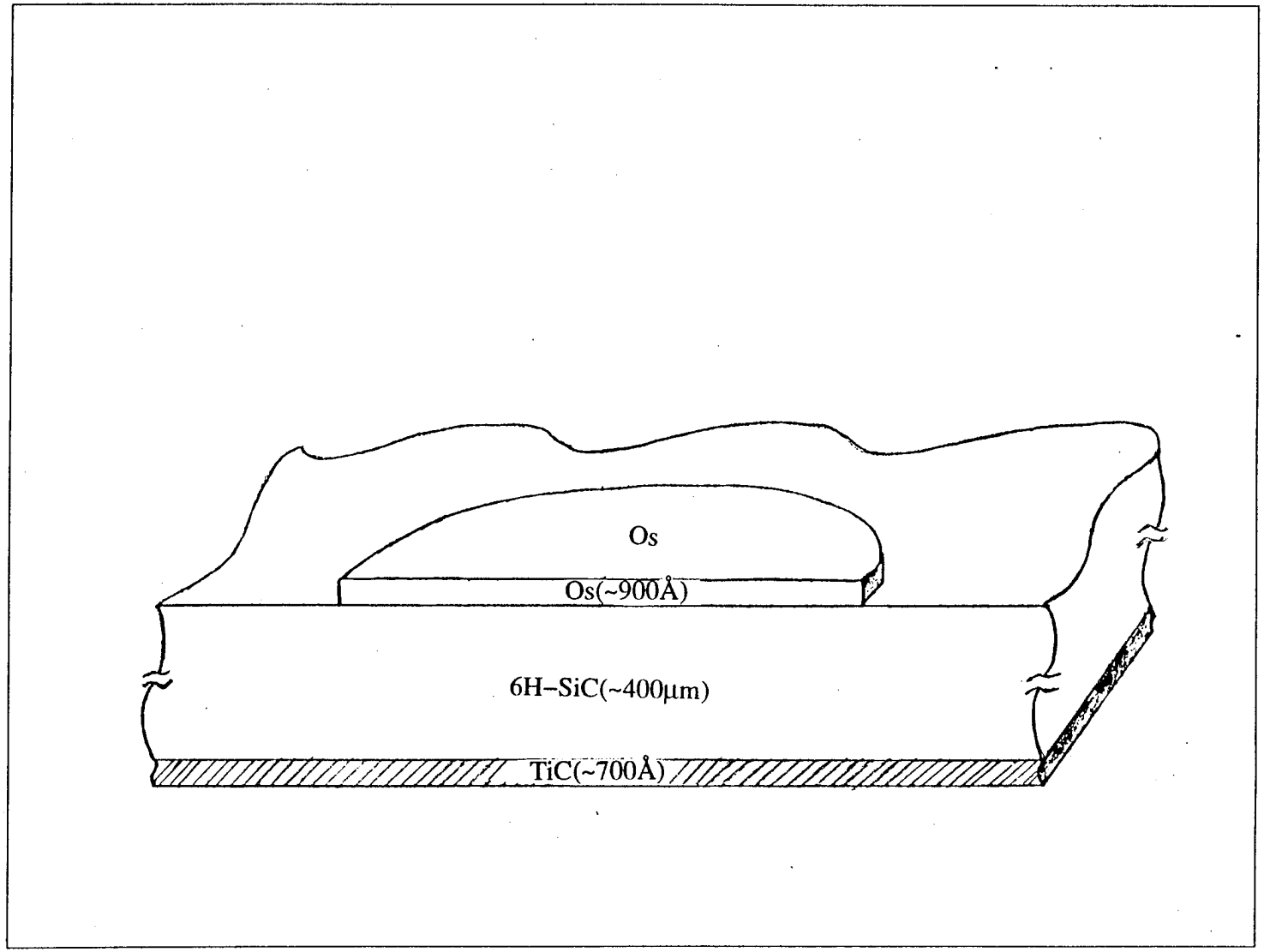



**Fig 1. Schematic representation of Schottky diode arrays (Type 2 structures) on samples A1-A5.**

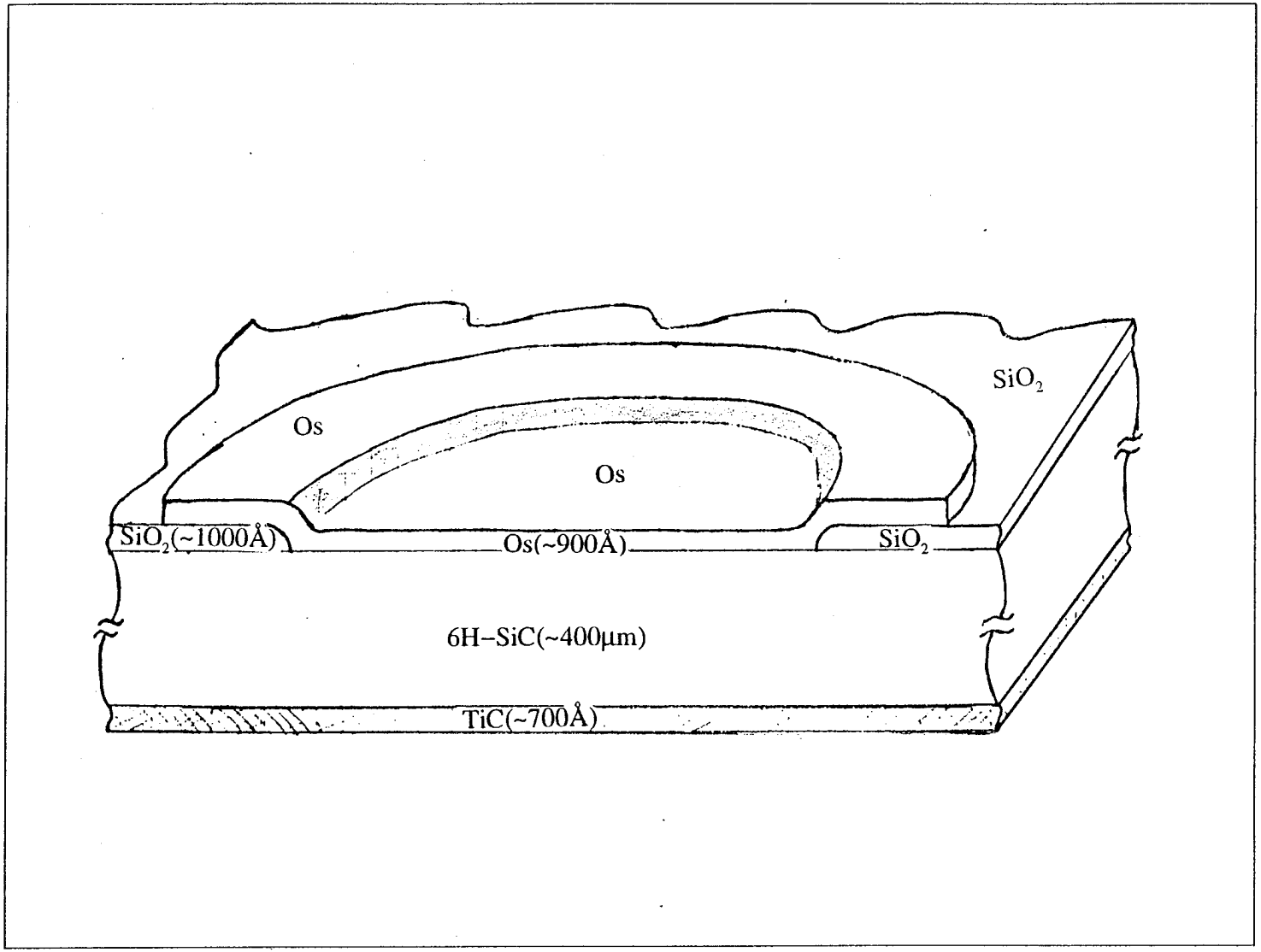
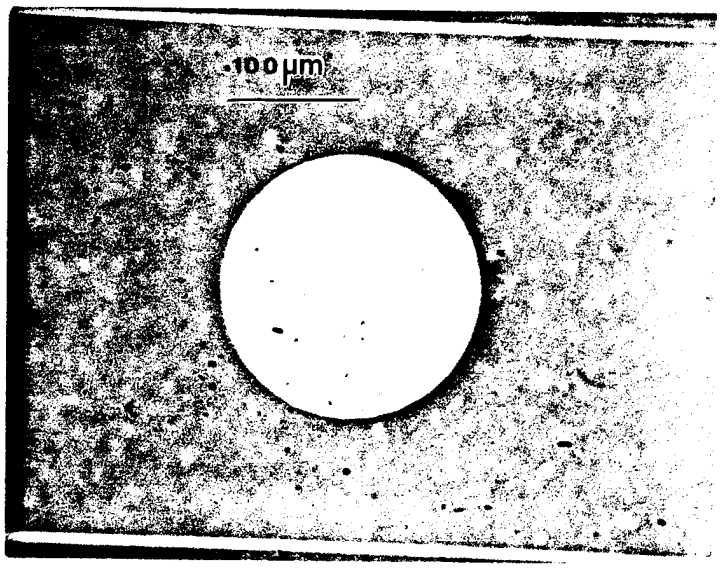



**Fig 2. Schematic representation of Schottky diode arrays (Type 3 structures) on samples D1 and D2.**

(a)

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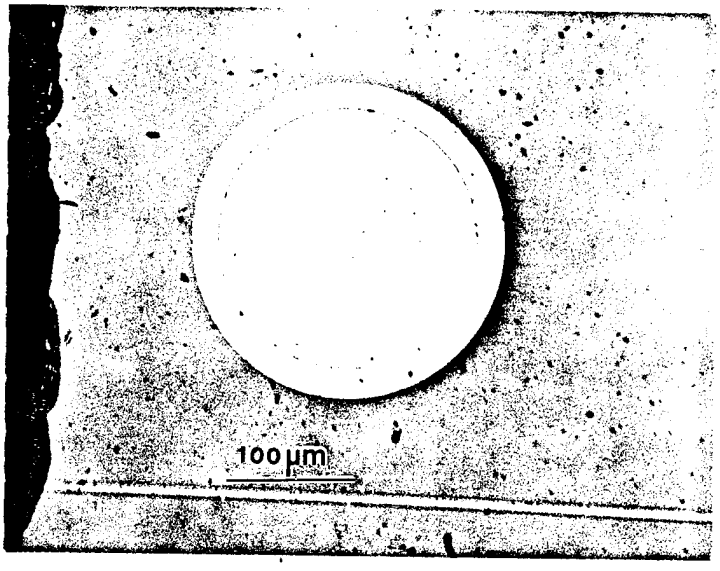


**Fig 3. Typical post lift-off Os dots on (a) SiC (Type 2 structures) and (b) on $SiC+SiO_2$ (Type 3 structures).**

## 3. Properties Versus Thermal Stress History

### Type 1 Structures:

The physical and electrical properties of Os films and the physical properties of Os/SiC junctions were investigated to:

- Determine the approximate temperature above which diffusion and chemical reactions occur at the Os/SiC interface.
- Determine the effects of Os surface exposure [gases (hydrogen & argon), materials ($SiO_2$, carbon & PBN)] on the Os/SiC annealing properties.
- Determine the approximate "forming" temperature of Os.

The resultant properties of Os films and Os/SiC junctions are presented as a function of annealing conditions in Table I. Analysis of these results are presented in Section 4.

**Table I. Type 1 structures: physical and electrical properties versus annealing conditions.**

| Annealing History | | | | Film and Interface Properties | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Sample No. | Os Surface (exposed to) | Each (min.) | Total (min.) | Temp. (°C) | Resistance (ohms)* | Adhesion (Os to SiC) | Os Surface (Nomarsky) | Os/SiC Junc (TEM) | Comments |
| ALL | | 0 | 0 | --------- | <170>** | Excellent | Specular | - | Light silver, mirror like surface, scratches with difficulty. |
| 2A | H(2)/H(2) | 60 | 60 | 1400 | <8000> | Excellent | Rough (Fig. 4) | - | Yellow-blue, grainy surface, very hard to scratch. |
| 3B | H(2)/H(2) | 60 | 60 | 1400 | <6000> | Excellent | Rough | - | Yellow-blue, grainy surface, extremely hard to scratch. |
| 4 | Ar/Ar | 60 | 60 | 1250 | <700> | Excellent | Rough | - | Silver-gray, fine textured surface, cannot scratch. (this surface was exposed to Ar: Fig. 5). |
| | PBN*** | 60 | 60 | 1250 | <24> | Excellent | Specular | - | Light silver, mirror like surface, scratches with difficulty. (this surface was in contact with PBN mask: Fig. 6) |
| 1C | Graphite/H(2) | 60 | 60 | 1100 | <13> | Excellent | Specular | - | Light silver, mirror like surface, scratches with difficulty. |
| | H(2)/H(2) | 60 | 120 | 1100 | <14.5> | Excellent | Texture | - | Light silver, texture visible @ 900x, scratches with difficulty. |
| | H(2)/H(2) | 30 | 150 | 1150 | <15> | Excellent | Texture | Reaction (Fig. 7) | Light silver, texture visible @ 130x, cannot scratch. *Osmium Thickness = 530 Å.* |
| 2B | Ar/Ar | 60 | 60 | 1100 | <25> | Excellent | Texture | - | Light silver, texture visible @ 900x, scratches with difficulty. |
| | H(2)/H(2) | 15 | 75 | 1200 | <11> | Excellent | Texture | - | Light silver, texture visible @ 440x, cannot scratch. |
| 3A | Graphite/H(2) | 60 | 60 | 1400 | <1000> | Excellent | Rough | - | Yellow-blue, crusty surface, very hard underneath. |
| 1A | H(2)/H(2) | 60 | 60 | 1100 | <35> | Excellent | Specular | - | Light silver, replicates substrate surface, very hard surface (this appears to be close to "forming" temperature) |
| | H(2)/H(2) | 30 | 90 | 1175 | <23> | Excellent | Texture | Reaction Figs.9 & 10 | Light silver, texture visible @ 900x, cannot scratch. *Osmium Thickness = 530 Å.* |
| 1B | H(2)/H(2) | 60 | 60 | 1100 | <24> | Excellent | Specular | - | Light silver, replicates substrate surface, very hard surface |
| | H(2)/H(2) | 30 | 90 | 1175 | <18> | Excellent | Texture | - | Light silver, replicates substrate surface, very hard, texture visible @ 900x. (some areas look as they did before this anneal: Fig. 8) |

Key: * Resistance measured between 2 tungsten probes on Os surface, probe separation about 100 microns.
** <#> represents average of several measurements.
*** PBN = pyrolytic boron nitride: used as a mask for mounting the structures in the annealing furnace.

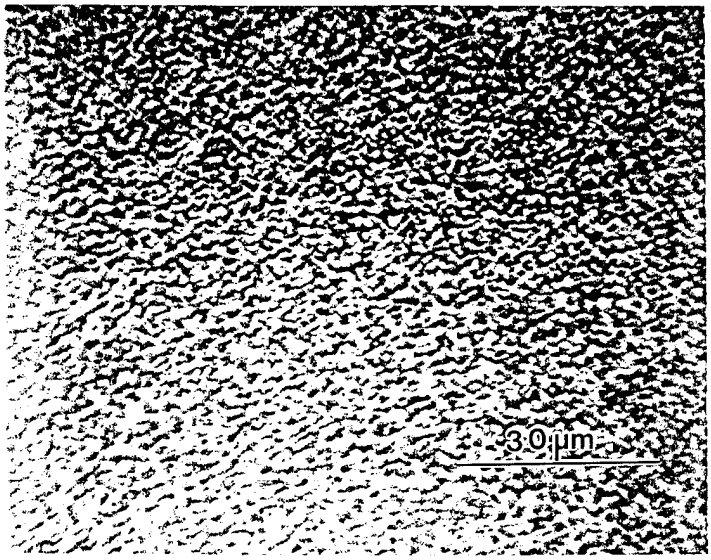


Fig. 4. Nomarsky micrograph (910x) of the Os surface of sample 2A after a 60 minute anneal at 1400°C in hydrogen. The Os was very hard (could not be scratched) and no evidence of spaling was observed. The roughness of the surface is due to chemical reaction at the Os/SiC junction.

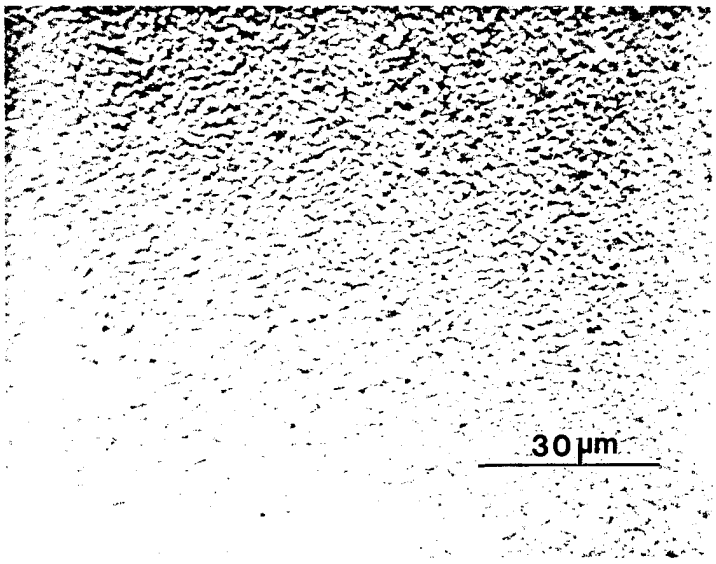


**Fig. 5. Nomarsky micrograph (910x) of Os surface of sample 4 after 60 min. exposure to Ar at 1250°C.**

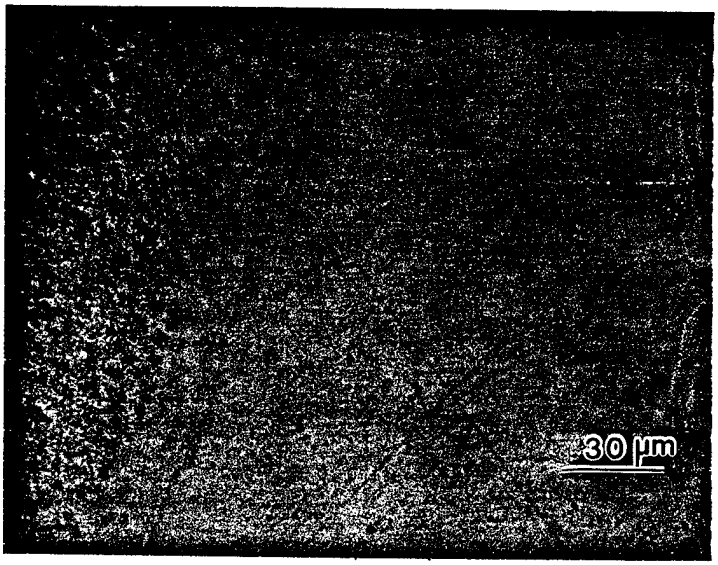


**Fig. 6. Nomarsky micrograph (440x) of Os surface of sample 4 after a 60 minute anneal at 1250°C; the textured Os surface on the left was exposed to Ar, the smooth Os surface on the right was in contact with PBN during the anneal.**

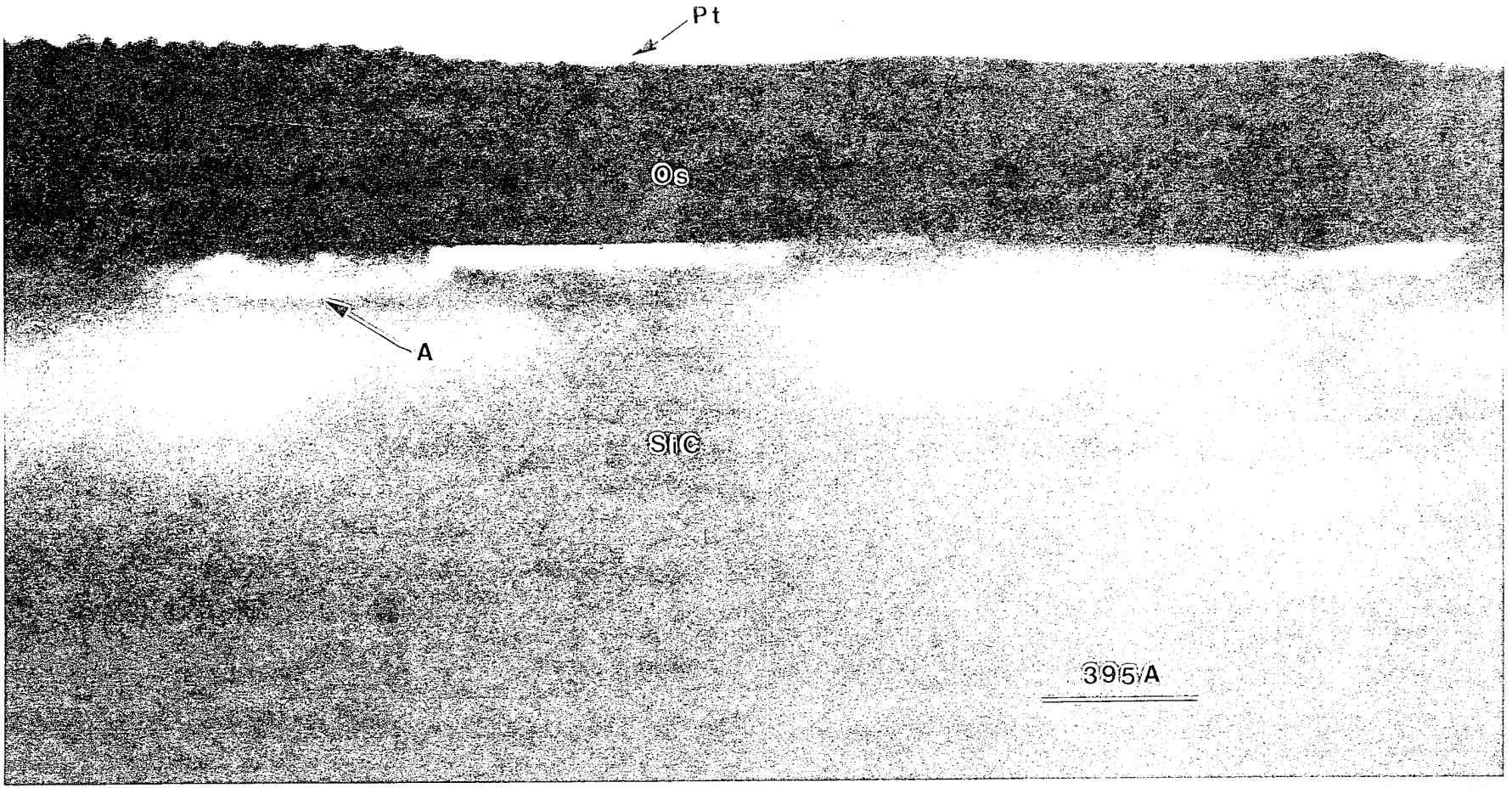


Fig. 7. TEM cross section of Os/SiC junction (sample 1C), after annealing at 1150°C, as described in Table I. A reaction between Os and Si is indicated by SiC lattice irregularities within about 20 Å of the Os interface (e.g. region A).

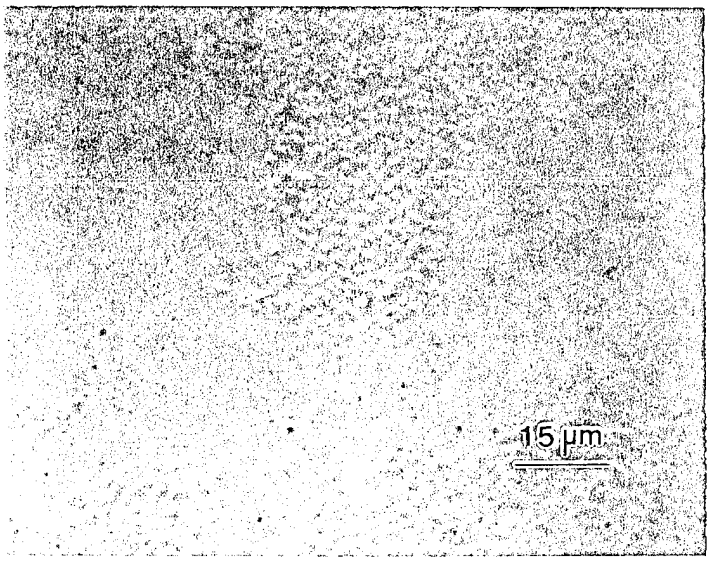


Fig. 8. Sample 1A (910x) showing smooth and rough areas of Os surface annealed at 1175°C, as described in Table I. The differences in Os morphology suggest that texturing (associated with reactions between Os and Si) may be influenced by SiC defect structure.

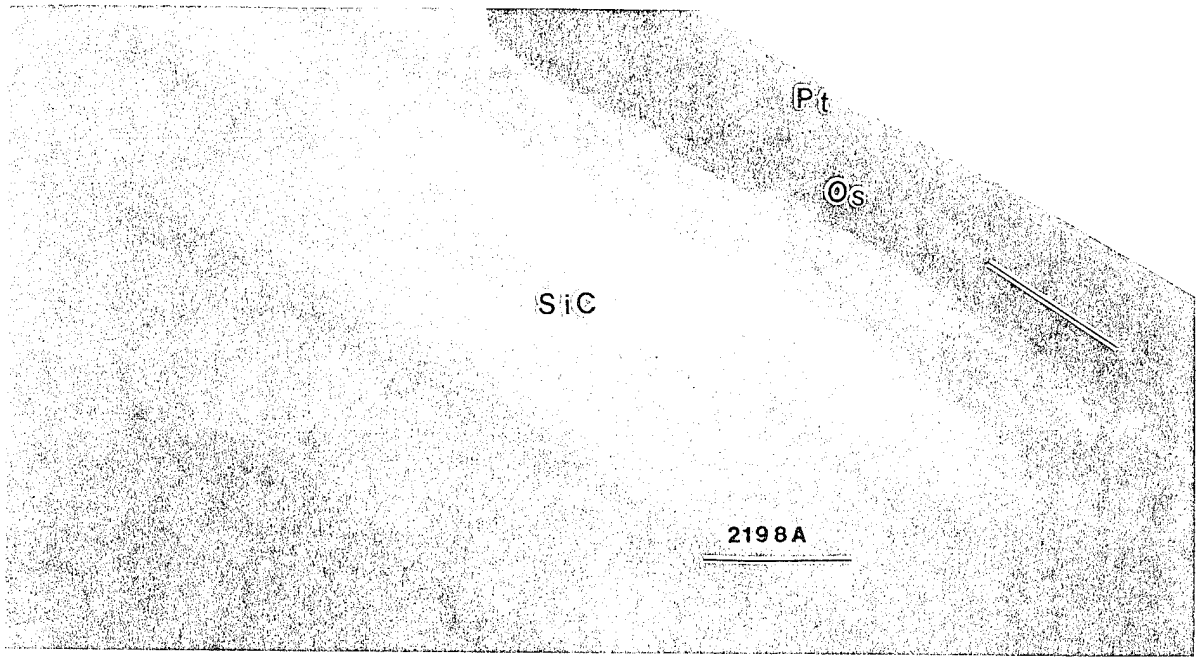


Fig. 9. TEM cross section of Os/SiC junction under rough surface region of sample 1A (see Fig. 8),after annealing at 1175°C, as described in Table I. The swirl patterns at the Os/SiC interface indicate strain, induced by the formation of an OsSi layer, mixed with free carbon.

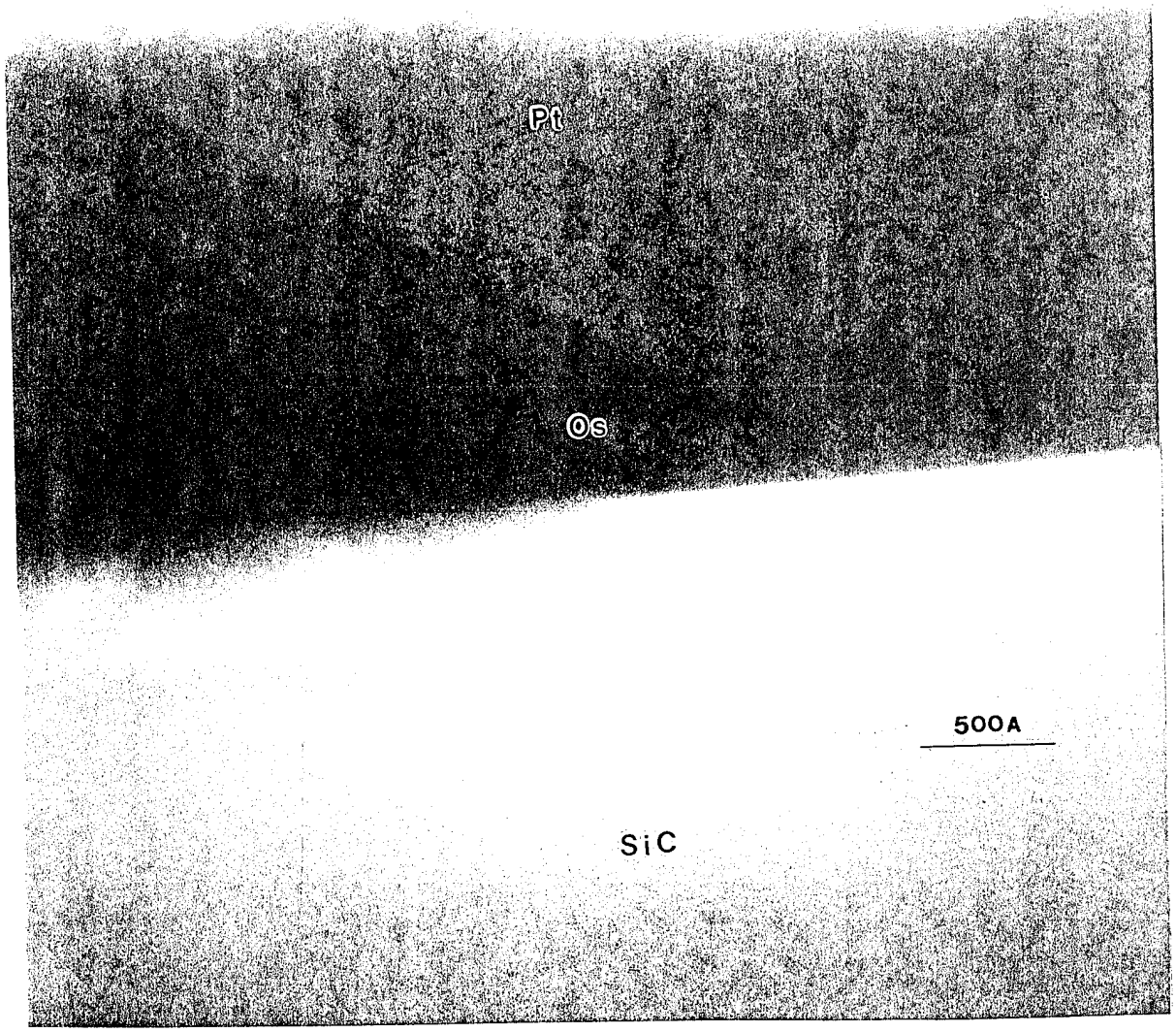


Fig.10. TEM cross section of Os/SiC junction under smooth surface region of sample 1A (see Fig. 8), after annealing at 1175°C, as described in Table I. This Os/SiC interface looks like the interface of sample 1C (Fig. 7).

## Type 2 Structures:

The physical properties of Os films and the physical and electrical properties of Os/n-SiC junctions were investigated to:

- Identify within ±25°C, the maximum temperature at which Os/SiC junctions remain essentially diffusion and reaction free.
- Investigate Os/SiC junction patchiness versus annealing temperature.
- Investigate the effects of Os-Si bonding reactions on Os/n-SiC junction properties.
- Determine the barrier height of Os / n-type 6H-SiC junctions.

**Table II. Type 2 structures: physical and electrical properties versus annealing conditions.**

| | ANNEALING* | | | PHYSICAL PROPERTIES 6H-SiC | | | Os/n-SiC JUNCTION ELECTRICAL PROPERTIES | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Diode | Time | | | | | | | | Measurec | Schottky | Total | Workfunction | | J(Reverse)^ | |
| Array | Each | Total | Temp. | Os Surface | Adhesion | Conc.** | CV Intercept | Built-In | Barrier | Lowering | Barrier | Os(effective) | J(Sat)**** | @ -1 Volt | Ideality |
| No. | (min.) | (min.) | (°C) | (Morphology) | (Os to SiC) | [n(cm*-3)] | (volts) | volts/eV | volts/eV | (volts/eV) | volts/eV | (volts/eV) | amps/cm*2 | amps/cm*2 | (<n>)~ |
| A1 | 0 | 0 | - | Specular | Excellent | 1.0±0.6e18 | *** | - | - | 0.13 | - | - | 5E-06 | 1E-04 | 1.34 |
| | 30 | 30 | 1100 | (Fig. 11) | Excellent | | ^^ | - | - | 0.13 | - | - | 1E-05 | 1E-02 | 1.31 |
| A2 | 0 | 0 | - | Specular | Excellent | 1.0±0.6e18 | *** | - | - | 0.13 | - | - | - | 2E-04 | - |
| | 30 | 30 | 1150 | (Fig. 12) | Excellent | | ^^ | - | - | 0.13 | - | - | 7E-05 | - | - |
| A3 | 0 | 0 | - | Specular | Excellent | 1.0±0.6e18 | *** | - | - | 0.13 | - | - | - | 1E-04 | - |
| | 40 | 40 | 1000 | Specular | Excellent | | *** | - | - | 0.13 | - | - | 4E-06 | 1E-02 | 1.07 |
| | 30 | 70 | 1050 | Specular | Excellent | | 1.47 | 1.50 | 1.62 | 0.13 | 1.74***** | 5.74 | 2E-05 | 1E-02 | 1.24 |
| | 30 | 100 | 1050 | Specular | Excellent | | 1.47 | 1.50 | 1.62 | 0.13 | 1.74***** | 5.74 | 5E-05 | 1E-02 | 1.26 |
| A4 | 0 | 0 | - | Specular | Excellent | 1.0±0.6e18 | *** | - | - | 0.13 | - | - | 1E-05 | 1E-04 | 1.41 |
| | 90 | 90 | 935 | Specular | Excellent | | *** | - | - | 0.13 | - | - | 5E-05 | 1E-03 | 1.14 |
| | 1 | 91 | 1030 | Specular | Excellent | | 1.75 | 1.78 | 1.90 | 0.13 | 2.02***** | 6.02 | 5E-05 | 1E-03 | 1.26 |
| A5 | 0 | 0 | - | Specular | Excellent | 1.0±0.6e18 | *** | - | - | 0.13 | - | - | 1E-05 | 5E-05 | 1.60 |
| | 30 | 30 | 700 | Specular | Excellent | | *** | - | - | 0.13 | - | - | 1E-05 | 5E-03 | 1.34 |
| | 2 | 32 | 950 | Specular | Excellent | | *** | - | - | 0.13 | - | - | 1E-05 | 2E-03 | 1.21 |
| | 2 | 34 | 975 | Specular | Excellent | | *** | - | - | 0.13 | - | - | 1E-05 | 2E-03 | 1.21 |
| | 30 | 64 | 1050 | Specular | Excellent | | 1.58 (Fig.16) | 1.60 | 1.72 | 0.13 | 1.84***** | 5.84 | 1E-05 | 2E-03 | 1.21 |

Key:

* All diode arrays annealed in H(2) atmosphere, Os surface exposed to H(2).

** Concentrations measured from slope of 1/(CxC), obtained from C-V measurements of 200 µm and 80 µm diameter Os/n-SiC diodes

*** Contact area less than diode area; built-in voltage cannot be extrapolated until Os/SiC contact area = Os dot area.

**** Barrier height = built-in + kT @ room temp (0.02526 eV) + [{E(conduction band)-E(Fermi)} (0.12 eV)].

***** The saturation current is field emission dominated; thus, the primary current mechanism is tunneling.

^ Reverse leakage current density measured at -1 volt.

^^ Only the 200 & 80 µm diam. diodes were large enough to negate fringe capacitance effects; all such diodes on these 6H-SiC substrates intercepted major defects.

~ Average of measurements from diodes of all diam. (20, 40, 80 & 200 µm).

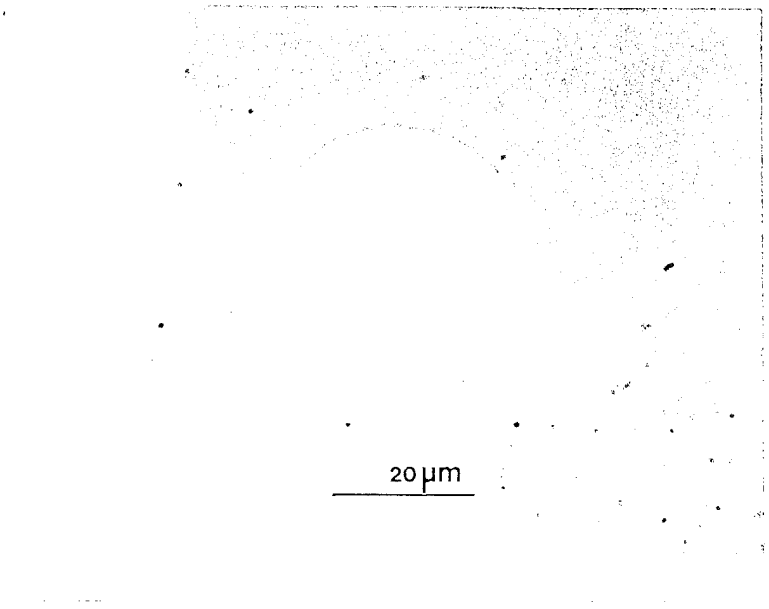


Fig.11. Nomarsky micrograph (910x) of Os diode surface (A1) after a 30 minute anneal in hydrogen at 1100°C; it has a very fine surface texture.

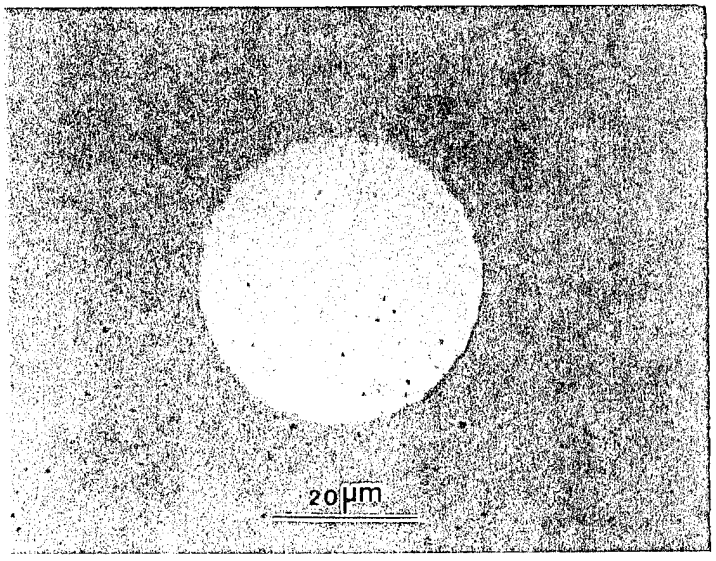


Fig.12. Nomarsky micrograph (910x) of Os diode surface (A2) after a 30 minute anneal in hydrogen at 1150°C, this surface is clearly rougher than the surface in Fig. 11.

## Type 3 Structures:

The physical properties of Os films on SiC and $SiO_2$, and the physical and electrical properties of Os/n-SiC and Os/$SiO_2$ junctions were investigated to:

- Determine the physical stability of Os/SiC and Os/$SiO_2$ junctions at 1050°C.
- Investigate the effects of Os-Si bonding reactions on Os/n-SiC junction properties.
- Investigate the effects of $SiO_2$ junction termination on Os / n-type 6H-SiC junctions.

Notes: The thicknesses of $SiO_2$ and Os were determined from TEM cross-sections of sample D1.

1. Thickness of thermally grown $SiO_2$ = 1600 Å
2. Thickness of 1050°C annealed Os = 640 Å.

**Table III. Type 3 structures: physical and electrical properties versus annealing conditions.**

| | ANNEALING* | | | PHYSICAL PROPERTIES | | | | | | 6H-SiC | Os/n-SiC JUNCTION ELECTRICAL PROPERTIES" | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Diode | Time | | | Os Surface | | Os Adhesion | | Interfaces | | | 1/C*2 vs V | | Meas. Schottky | | Total | Work Func. | | | J(reverse)^ | |
| Array | Each | Total | Temp | on | on | to | to | TEM Cross-Sections | | Conc.** | Intercept | Built In | Barrier | Lower | Barrier | Os(effec.) | J(Sat)***** | | @ -1 Volt | Ideality |
| No. | min. | min. | (°C) | 6H-SiC | SiO(2) | 6H-SiC | SiO(2) | Os/SiC | Os/SiO(2) | [n{cm*-3)] | (volts) | volts/eV | volts/eV | volts/eV | volts/eV | (volts/eV) | amps/cm*2 | | amps/cm*2 | (<n>)~ |
| D1 | 0 | 0 | - | Spec | Spec | Excel | Excel | Abrupt | Abrupt | ? | ? | ? | ? | ? | ? | ? | ? | | ? | - |
| | 40 | 40 | 1050 | Spec | Spec | Excel | Excel | Abrupt | Abrupt | ? | ? | ? | ? | ? | ? | ? | ? | | ? | - |
| | | | | | | | | Figs.13&14 | Figs.14&15 | | | | | | | | | | | |
| D2 | 0 | 0 | - | Spec | Spec | Excel | Excel | - | - | 1.0±0.6E18 | *** | - | - | - | - | - | 4.0E-06 | | 2.0E-04 | 1.30 |
| | 30 | 30 | 900 | Spec | Spec | Excel | Excel | - | - | | *** | - | - | - | - | - | - | | - | - |
| | 30 | 60 | 950 | Spec | Spec | Excel | Excel | - | - | | *** | - | - | - | - | - | - | | - | - |
| | 30 | 90 | 975 | Spec | Spec | Excel | Excel | - | - | | *** | - | - | - | - | - | 4.0E-06 | | 8.0E-04 | 1.25 |
| | 30 | 120 | 1050 | Spec | Spec | Excel | Excel | - | - | | 1.75 (Fig.16) | 1.78 | 1.90**** | 0.13 | 2.02 | 6.02 | 4.0E-06 | | 2.0E-04 | 1.24 |

Key:

* All diode arrays annealed in H(2) atmosphere, Os surface exposed to H(2).

** Concentrations obtained from C-V measurements of 200 µm and 80 µm diameter diodes without SiO(2) rings.

*** Contact area less than diode area; built-in voltage cannot be extrapolated until Os/SiC contact area = Os dot area.

? Substrate seems to contain deep levels, it exhibited n & p type characteristics, could not form electrical contact.

**** Barrier height = built-in + kT @ room temp (0.02526 eV) + [{E(conduction band)-E(Fermi)} (0.12 eV)].

***** The saturation current is field emission dominated; thus, the primary current mechanism is tunneling.

^ Reverse leakage current density measured at -1 volt.

^^ Only the 200 & 80 µm diam. diodes were large enough to negate edge capacitance effects; in these samples all diodes of these sizes intercepted major defects in the SiC substrates.

~ Average of measurements from diodes of all diam. (20, 40, 80 & 200 µm).

"C-V data obtained from Type 2 structures, I-V data obtained from Type 3 structures.

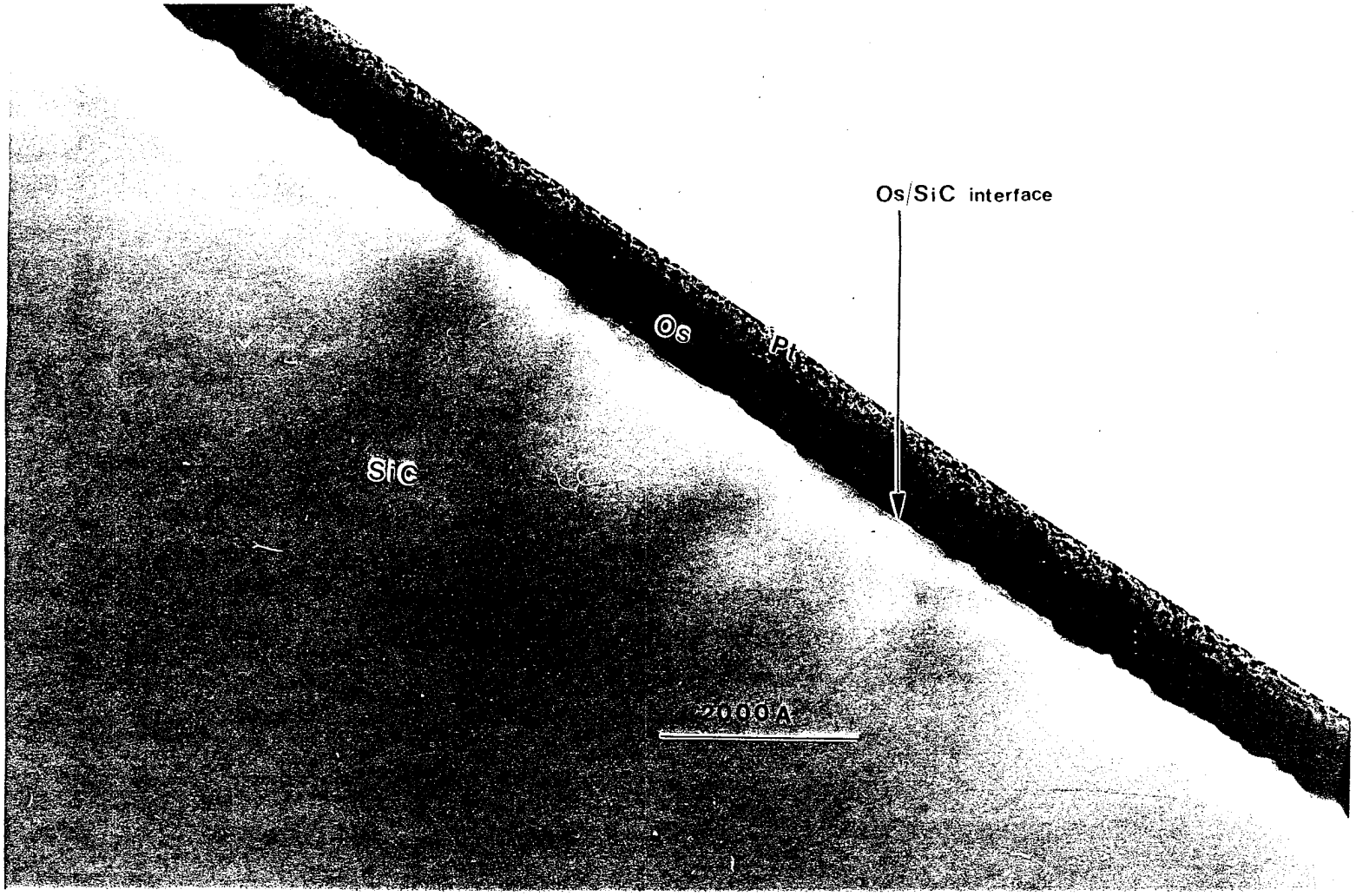


Fig.13. TEM cross-section of Os/SiC interface of sample D1 (annealed at 1050°C as described in Table III). The Os/SiC interface is the straight line just below the black irregular surface. The irregularity is caused by spreading of the Ga focused ion beam (FIB), which was used to thin the specimen for TEM investigation. The light and dark shadows in the SiC appear because the angle of observation is not aligned with a zone axis.

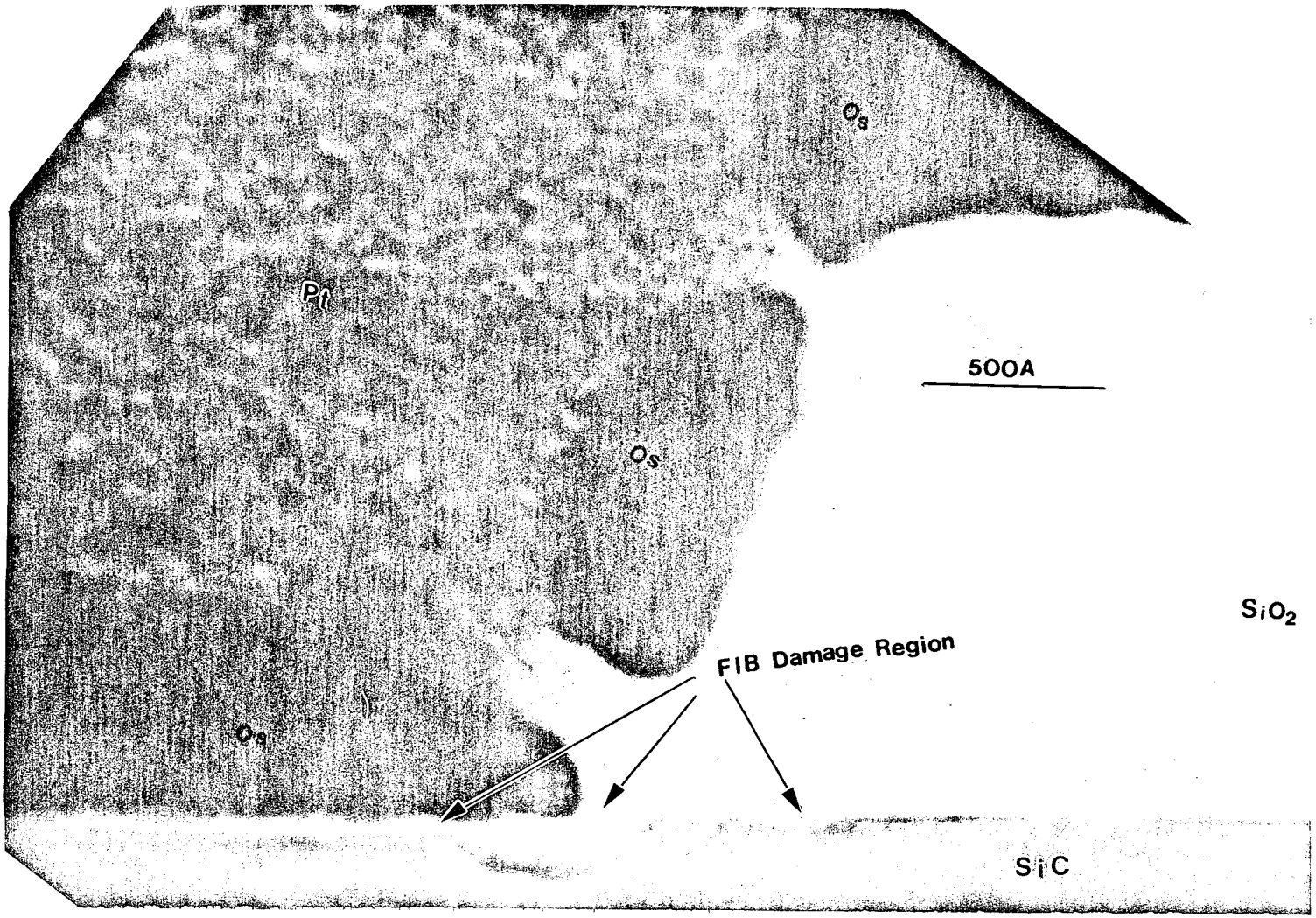


**Fig.14. TEM cross-section of Os/SiC interface (left), Os/$SiO_2$ interfaces (upper center and right) and SiC/$SiO_2$ interface (center right). Several important features are shown in this x-sec. of sample D1 (annealed at 1050°C, as described in Table III):**

1. **Their are gaps in the as-sputtered Os, at the high curvature positions of the side wall of the $SiO_2$ field ring.**
2. **The effect of the FIB beam spreading on interface damage is clearly evidenced by observing that the white region between the Os and SiC also extends throughout the SiC/$SiO_2$ interface; where, significant FIB damage can be seen in the SiC at the SiC/Os/$SiO_2$ junction.**
3. **The interfaces formed with SiC do not show any evidence of chemical reaction.**

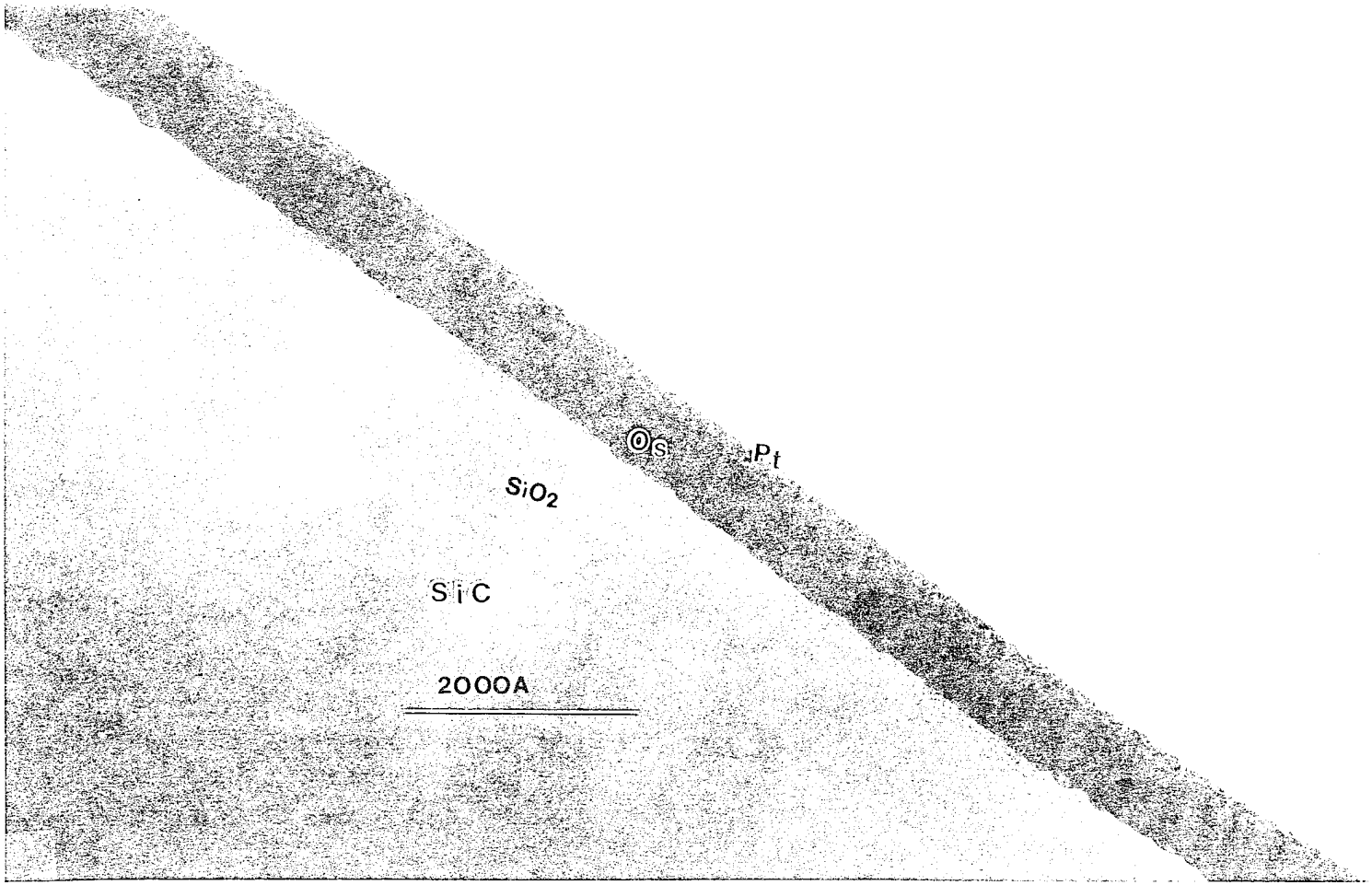


Fig.15. TEM cross-section of $Os/SiO_2$ and $SiC/SiO_2$ interfaces of sample D1 (annealed at 1050°C, as described in Table III). The apparent roughness of the $Os/SiO_2$ interface is due to vapor transport and redeposition of the Os by a too high density FIB; redepositions of Os on the TEM face of $SiO_2$ can be seen e.g. at region A.

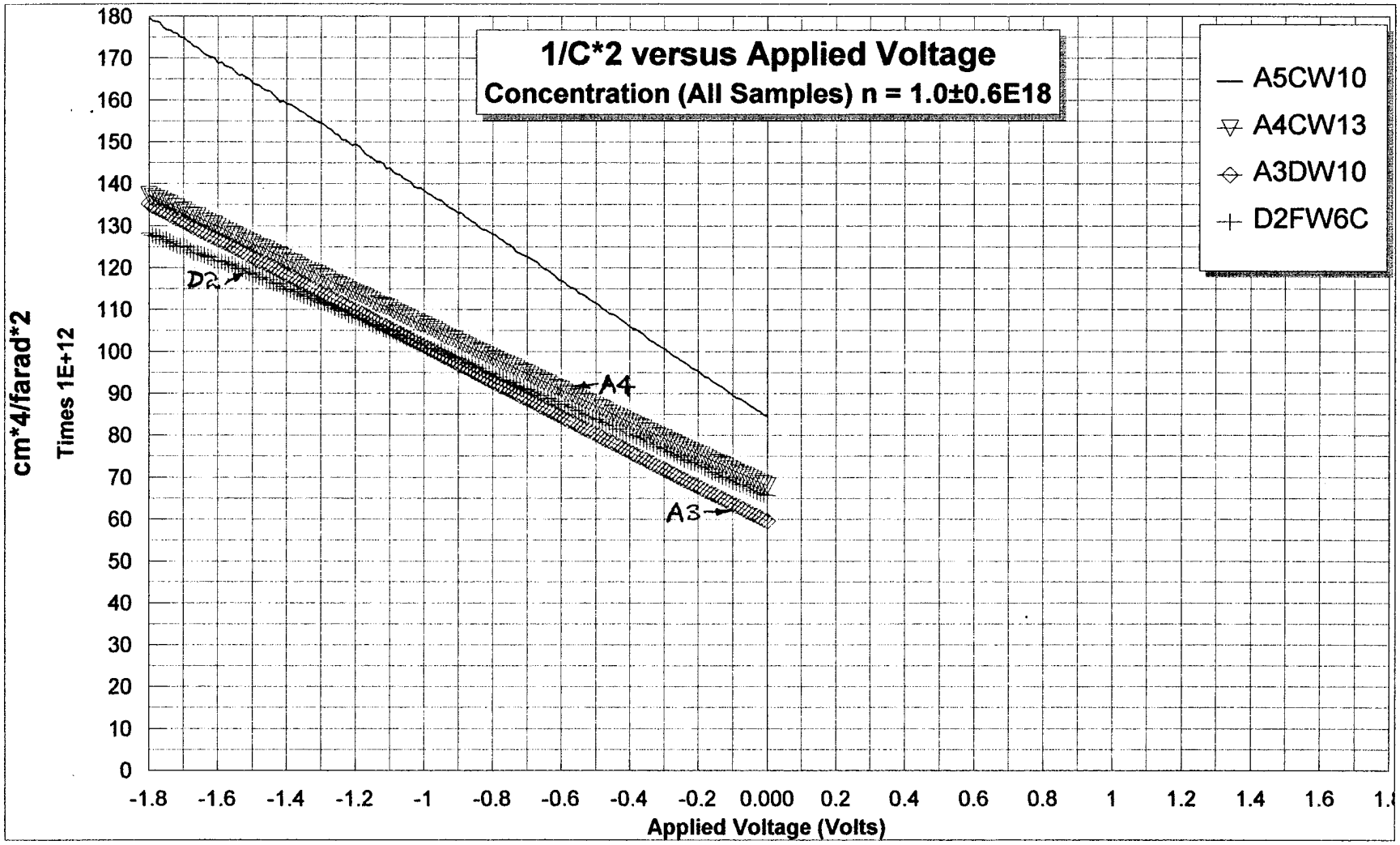


**Fig.16. Representative $1/C^2$ vs voltage curves used to determine the intercept voltages used for barrier height calculations. Note that the C-V curves obtained from sample D2 were measured on diode structures without $SiO_2$ guard rings.**

## 4. Analysis

### 4.1. Adhesion of Os to SiC and $SiO_2$:

15 - 1050°C: Os did not spall or delaminate. could not be peeled with scotch tape and was extremely difficult to scratch on both surfaces.

1050 - 1400°C: Os on SiC did not spall or delaminate, could not be peeled with scotch tape and was almost impossible to scratch.

### 4.2. Forming Temperature = Temperature required to crystallize as-sputtered Os:

The changes in Os thickness as a function of annealing temperature, and the observation of grain boundaries, indicate that the minimum forming temperature is >=700°C. At or above 700°C Os densifies (as-sputtered layer thickness decreases) at a measurable rate; where, the forming rate increases with increasing temperature.

The thickness of fully densified ('formed') Os films is approximately 70% of the as-sputtered thickness. This is extrapolated from TEM measurements of Os films annealed at 1050°C [sample D1 640 Å)], 1150°C [1C (530 Å)] and 1175°C [1A (530 Å)], and noting that part of the Os film thickness of samples 1A and 1C was removed during FIB processing, because the Pt mask was complete gone.

### 4.3. Os/SiC Interface: Patchiness, Thermal Stability and Chemistry:

**4.3.1. Patchiness:** This is fraction of the Os surface that is in intimate contact with SiC. Changes in C-V data obtained from specific diodes, as a function of annealing temperature, indicate that annealing should be performed at 1030°C for at least 1 minute to insure that the actual contact area = the diode area. We anticipate that longer times at lower temperatures will also work.

**4.3.2. Thermal Stability:** TEM and electrical results indicate that Os in contact with SiC forms an abrupt, chemically stable junction to at least 1050°C. Os morphological changes at 1100°C suggest that the maximum temperature at which the Os/SiC junction remains abrupt and chemically stable is 1050°C <= T < 1100°C.

**4.3.3. Chemistry:** Comparison of reverse current measurements as a function of annealing temperature in Type 2 and Type 3 structures suggests that when Os bonds to SiC, a few monolayers of free carbon (<10Å from TEM) is formed. This thin free C layer forms a leakage current path around the edges of the diodes.

Type 2 and Type 3 structures exhibited increased reverse currents when annealed above 700°C for as little as 1 minute. Thereafter, the reverse current was not changed by annealing at temperatures up to 1050°C in Type 2 structures; however, the reverse current returned to its pre-anneal value in Type 3 structures when they were annealed at temperatures between 1030 and 1050°C.

The recovery of the Type 3 structures is thought to be due to reaction between C and $SiO_2$ to form trapped $CO_2$. Thus, the very simple solution to the free C formation is to deposit a few monolayers (only 1 is required) of Si on the SiC just before the Os is deposited. This should yield Os/SiC junctions in Type 2 and Type 3 structures with reverse current properties which are impervious to temperatures at least as high as 1050°C.

**4.4. Os/$SiO_2$ Interface:** This interface appears to be stable to at least 1050°C (the maximum temperature at which it was tested). Up to 1050°C, the Os surface morphology and TEM cross-sections indicate that no reactions are occurring.

**4.5. Sample Preparation Effects on TEM Analysis:** The quality of the TEM cross-sections was degraded by two factors: (1) Pt mask thickness and (2) non-parallel character of the Ga focused ion beam (FIB) used for final thinning of the TEM sections. The effects of these factors is shown in Figs.17 and 18.

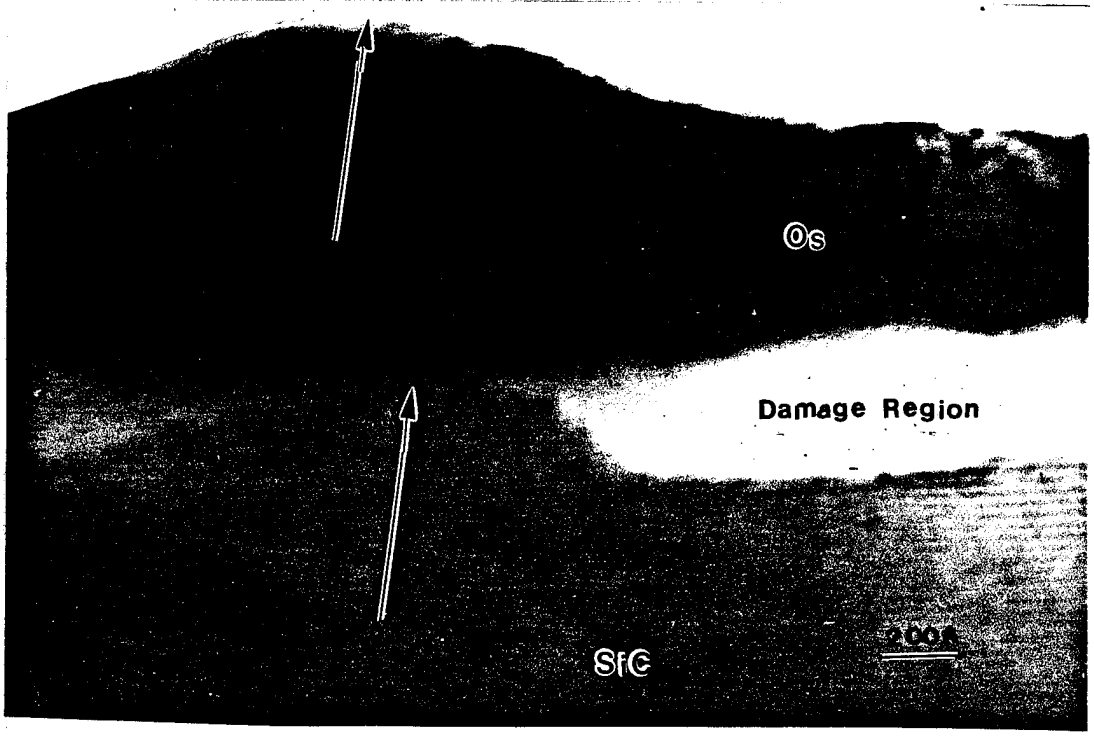


**Fig.17. TEM cross-section showing ion bombardment damage to the Os/SiC interface via ions passing through the Os; note that the damaged (white) region gets thinner as the Os gets thicker. A thicker Pt mask would clearly solve this problem.**

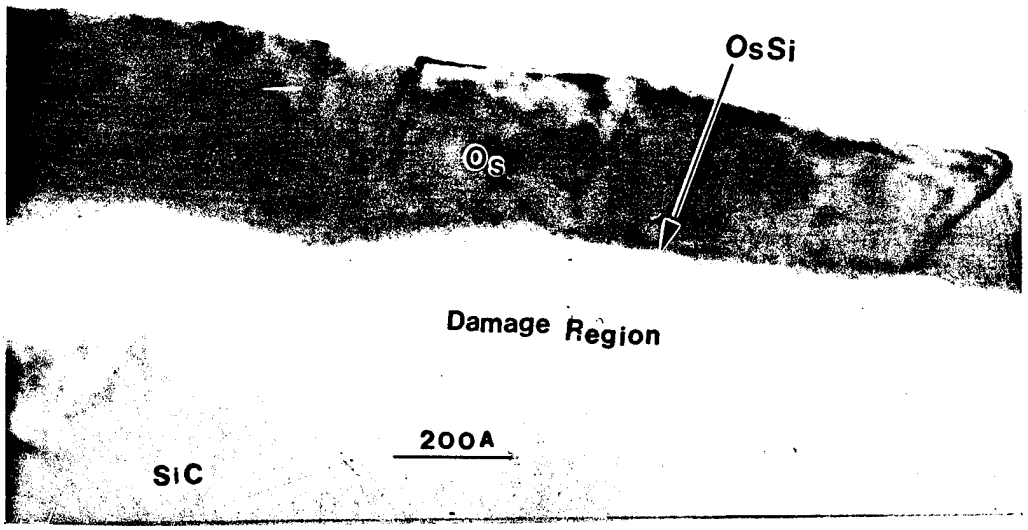


**Fig.18. TEM cross-section of sample 1A (annealed at 1175°C), showing side-wall damage due to spreading of the FIB (white region), a thin reaction layer between the damaged region and the Os. Note that the grain boundaries in the Os layer (this means that it is completely 'formed').**

### 4.6. Electrical Properties of Os / n-Type 6H-SiC Junctions [Summarized in Table IV]:

Definitions of Symbols and Terms:

| | | |
|---|---|---|
| $1/C^2$ vs applied voltage intercept with the voltage axis ..... | | = V(I). |
| Built-in voltage = V(I) + kT/q ..... | $= \Phi_{bi}$ | = V(bi). |
| Measured barrier voltage = V(bi) + Fermi Voltage $\{E_f/q\}$ ..... | $= \Phi_{bn}$ | = V(bn). |
| Schottky barrier lowering voltage ..... | $= \Delta\phi_{Sch}$ | = V(S). |
| Total barrier in the absence of Schottky barrier lowering = V(bn) + V(S) ... | | = V(t). |
| Osmium work function voltage = V(t) + SiC electron affinity voltage $\{\chi_e\}$ .. | $= \Phi_M$ | = V(M). |
| Junction ideality factor ..... | | = n. |
| Depletion Layer Depth from Metallurgical Junction ..... | $= x_D$ | = x(D). |

**Table IV. Averaged Os/n-SiC junction electrical properties used to construct energy band model.**

| Diode Array No. | ANNEALING Temperature Maximum (°C) | PHYSICAL PROPERTIES Os Surface on 6H-SiC | Os Surface on SiO(2) | Os Adhesion to 6H-SiC | Os Adhesion to SiO(2) | 6H-SiC Conc. [n{cm*-3}] | Os/n-SiC JUNCTION ELECTRICAL PROPERTIES 1/C*2 vs V Intercept (volts) | Built In volts/eV | Meas. Barrier volts/eV | Schottky Lower volts/eV | Total Barrier volts/eV | Work Func. Os(effec.) (volts/eV) | J(Sat)* amps/cm*2 | Ideality (<n>) | Depletion Depth** (Å) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| A3 | 1050 | Spec | Spec | Excel | Excel | 1.0±0.6E18 | 1.47 | 1.50 | 1.62 | 0.13 | 1.74 | 5.74 | 5.0E-05 | 1.26 | - |
| A4 | 1030 | Spec | Spec | Excel | Excel | 1.0±0.6E18 | 1.75 | 1.78 | 1.90 | 0.13 | 2.02 | 6.02 | 5.0E-05 | 1.26 | - |
| A5 | 1050 | Spec | Spec | Excel | Excel | 1.0±0.6E18 | 1.58 | 1.60 | 1.72 | 0.13 | 1.84 | 5.84 | 1.0E-05 | 1.21 | - |
| D2 | 1050 | Spec | Spec | Excel | Excel | 1.0±0.6E18 | 1.75 | 1.78 | 1.90 | 0.13 | 2.02 | 6.02 | 4.0E-06 | 1.24 | - |
| ***Average*** | **-** | ***Spec*** | ***Spec*** | ***Excel*** | ***Excel*** | ***1.0±0.6E18*** | ***1.64*** | ***1.66*** | ***1.78*** | ***0.13*** | ***1.91*** | ***5.91*** | ***2.9E-05*** | ***1.24*** | ***438*** |

* The saturation current density [J(sat)] is predominantly tunneling current, because of the high carrier concentrations of the 6H-SiC substrates.
** Calculated depletion depth at zero applied voltage.

**4.6.1. Intercept Voltage [V(I)]:** The accuracy of V(I) is critical, because all barrier parameter values are based upon it. Type 2 structure diodes (diam. = 80 μm and 200 μm) were used exclusively for this measurement. The fringing capacitance of smaller diameter diodes was to large, relative to the total capacitance, to obtain reliable V(I) data. The capacitance of the annular oxide ring on Type 3 structure diodes prevented their use for V(I) measurements. Annealing and capacitance measurements were itteratively performed until the capacitance stabilized; thus, indicating that the contact patchiness had been eradicated (diode area = Os/n-SiC contact area).

Typical $1/C^2$ vs V plots, as shown in Fig. 16, show that the curves are essentially linear and are within 30% each other. These curves show that the abrupt junction model should be used to calculate junction band structure parameters. The averaged V(I) is accurate to ±0.1volt. The junction band structure for these samples, determined from V(I) measurements, is shown in Fig. 19.

**4.6.2. Measured Barrier [V(bn)] and Schottky Lowering [V(S)] Effects on Junction Properties:** The measured value of V(bn) was 1.78 volts. The value of V(S) [0.13 volts] is based on the relative dielectric constant (10) and doping concentration ($n=1x10^{18}cm^{-3}$) of the 6H-SiC substrates. The conduction band in Fig. 19 is shown to terminate at the metallurgical junction, at 1.91 eV (1.91eV/q = 1.91 volts). However, the conduction band should bend downward at some point near the metallurgical junction. The position at which the conduction band edge reverses slope is the position at which V(bn) actually occurs - approximately 10 Å from the metallurgical junction, within the depletion region.

**4.6.3. Osmium Work Function Voltage [V(M)]:** The V(M) determined for Os from these measurements is 5.91 volts. This is very close to the published photoelectric measurement of 5.93 volts. This indicates that the effect of interface states on the Os/n-SiC barrier is vanishingly small.

**4.6.4. Current-Voltage Measurements:** The standard thermionic emission theory does not apply to these diodes because the principal current is due to field emission, through the barrier. This makes the results obtained with Os even more impressive. Any other metal would have yielded essentially a tunnel junction ohmic contact. The high 6H-SiC doping significantly affected two measurements: (1) the measured saturation current density is several orders of magnitude higher than it would be if the substrate doping were reduced by an order of magnitude (because of reduced emission current, resulting from wider x(D); and (2) the ideality factor would be much lower.

The ruggedness of the Os/n-SiC Schottky diode is illustrated by comparing I-V curves obtained from a sample D2 diode before annealing (Fig. 20) and after annealing at 1050°C for 30 min. (Fig. 21).

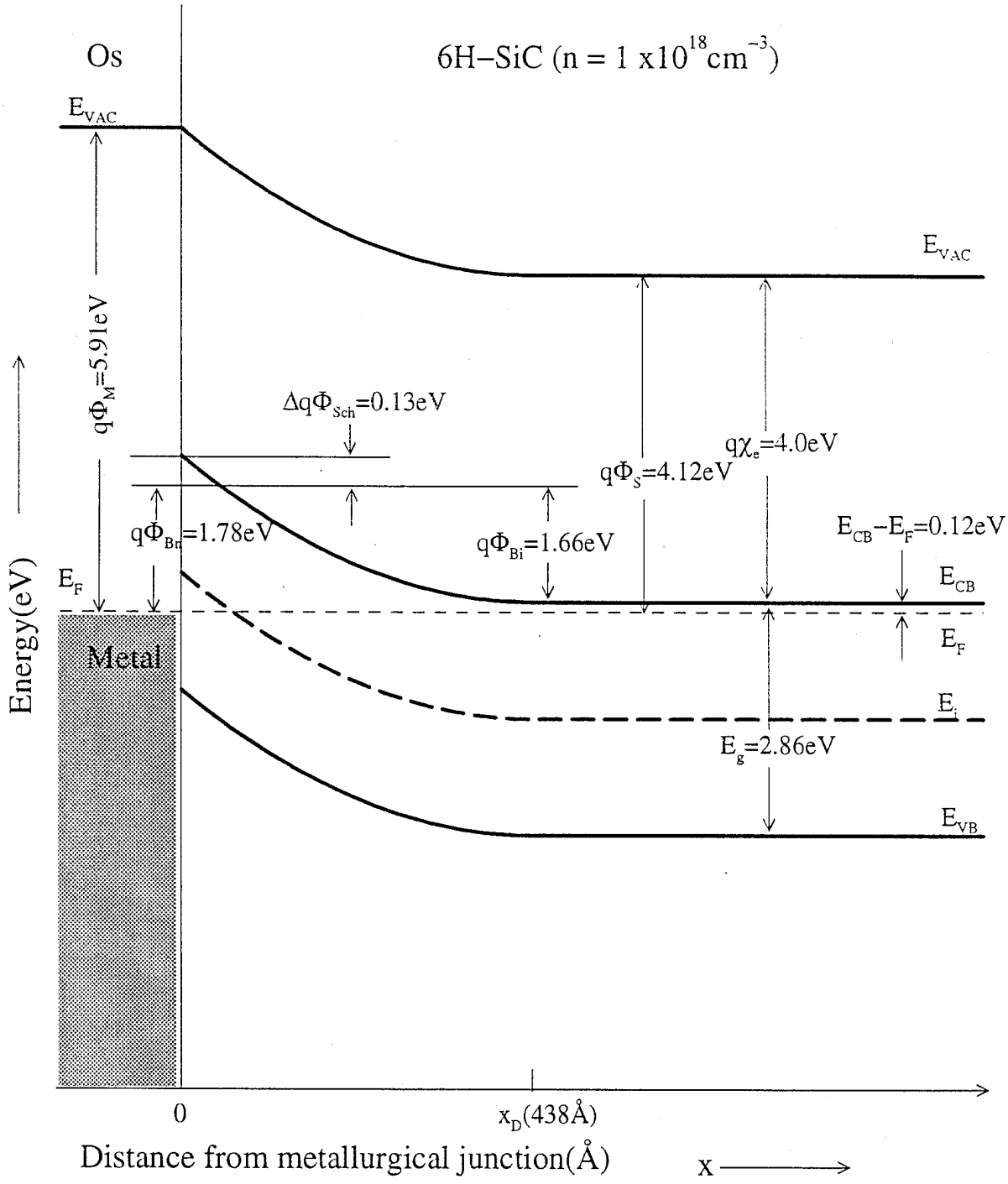


**Fig.19. Band structure of Os / n-type 6H-SiC junction determined from electrical and physical measurements of Schottky junctions.**

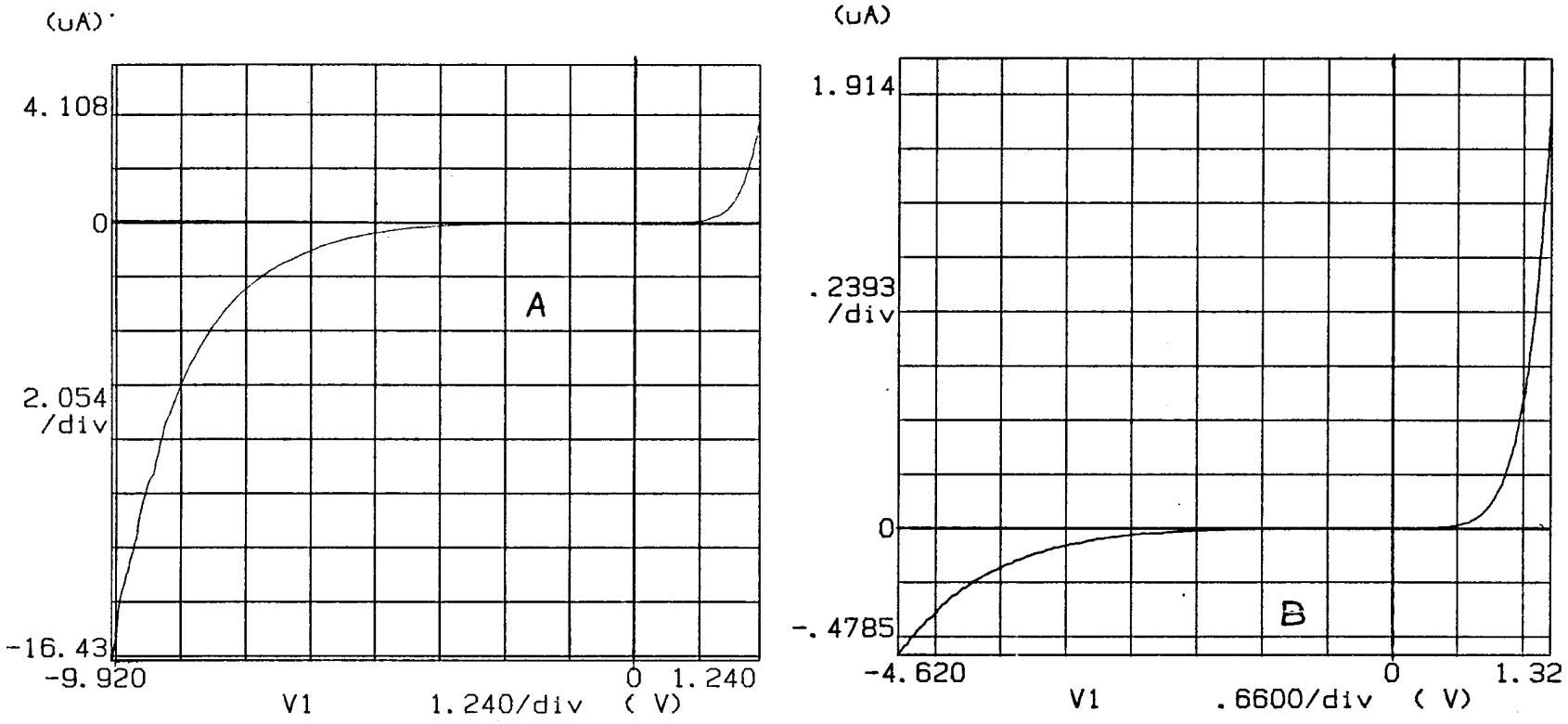


**Fig.20. Sample D2 diode (Type 3) I-V: curve (a) as-sputtered and curve (b) after annealing at 900°C (30 min) + 950°C (30 min) + 975°C (30 min) + 1050°C (30 min).**

## 5. Summary of Results and Conclusions

### 5.1. Summary of Results:

Adhesion:
- Os to SiC: Does not spall, delaminate, peel or scratch at 15°C<=T<=1050°C.
- Os to $SiO_2$: Does not spall, delaminate, peel or scratch at 15°C<=T<=1050°C.

Forming:
- Os forms (fully crystallizes/densifies) at temperatures greater than 700°C.

Patchiness:
- Os/SiC Interface: Complete interface contact obtained by 1 min. anneal at 1030°C.
- Minimum anneal temperature = 700°C, time not yet determined.

Interface Stability:
- Os/SiC: Abrupt junction, which is stable - indefinitely - up to 1050°C<T<1100°C.
- Os to $SiO_2$: Abrupt junction, which is stable - indefinitely - up to at least 1050°C.

Interface Chemistry:
- Os forms a chemical bond to SiC at T<= 1050°C, but 1 or 2 monolayers of free carbon is formed during this bonding process.
- Free carbon © provides a current leakage path at the edge of the Os/SiC junctions.
- The free C can be removed from the diode edges by reaction with $SiO_2$ to form $CO_2$ at 1030° for at least 1 minute.
- The formation of free C can be eliminated by depositing 1 or more monolayers of Si on SiC before performing the Os deposition.
- Os forms an interface with $SiO_2$ that is stable to at least 1050°C.

Electrical Properties of Os / n-Type <0001> 6H-SiC ($n=1\pm0.6x10^{18}cm^{-3}$) Junctions:

- Built-in voltage = 1.66 volts.
- Barrier height = 1.78 volts.
- Os work function voltage based on our measurements = 5.91 volts.
- Depletion layer depth at zero bias = 438 Å.
- Saturation current is predominantly emission (tunneling) due to high doping of 6H-SiC.
- Ideality factor, though measured from emission current, is very low (1.24).
- The junction I-V characteristics are not degraded by exposure to temperatures as high as 1050°C.

### 5.2. Conclusions:

The mechanical, thermal and electrical properties of Os rectifying Schottky barrier contacts to n-type SiC are superior to all other contact metals. Further, Os forms an electron transparent diffusion barrier which protects its junction with SiC from circuit and bonding metals at temperatures at least as high as 1050°C.

The results obtained in this feasibility study clearly show that the characteristics of Os/n-SiC Schottky junctions; where, the SiC n-type doping is $<= 1x10^{17}cm^{-3}$, will be superior to any alternative. Further, that such junction will not place any limitations on the thermal or power capabilities of SiC itself. The characteristics of the Os and its junction to n-type 6H-SiC were superior to predictions in the proposal in every respect.

## 6. Deliverables

Sample A5 and D2 are being sent to Dr. Christian Fazi with this report. All documentation and data on all processing and measurements will be provided upon request.